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10/684,939	10/14/2003	Keiji Mabuchi	09792909-5698	7761
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INGHAM, JOHN C				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/684,939

Applicant(s)

MABUCHI, KEIJI

Examiner

JOHN C. INGHAM

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 July 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 2, 4-9, 16, 17 and 19-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4-9, 16, 17 and 19-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 June 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1, 2, 4-8, 16, 17, 19-23 and 27-33** are rejected under 35 U.S.C. 102(b) as being anticipated by Fox (US 6,566,697, previously cited).

3. Regarding claims **1 and 16**, Fox discloses in Fig 1 a camera apparatus for outputting an image taken by a solid-state imaging device (col 2 In 1-6), the camera apparatus comprising: the solid-state imaging device having an imaging region section (10) provided with a plurality of pixels and a processing circuit section for processing an image signal output from the imaging region section (col 1 In 20-30), the solid-state imaging device comprising:

each pixel having a photoelectric converting element (12) which generates a signal charge commensurate with a light-receiving amount,

a charge holding region (18) of a second conductivity type (Fig 8 n-type region between TCK and RST) which holds a signal charge,

a transfer transistor (16) and gate insulation film (Fig 8, TCK) which transfers a signal charge generated by the photoelectric converting element to the charge holding region and has a threshold channel potential for turning on the transfer transistor which

is set to a value higher than a potential which depletes the photoelectric converting element (Fig 3B, col 8 ln 60-61, photosite is fully depleted through transfer transistor),

a drain transistor (22) and gate insulation film (Fig 8, EC) which drains a signal charge generated by the photoelectric converting element and has a threshold channel potential for turning on the drain transistor which is set to a value higher than a potential which depletes the photoelectric converting element (Fig 3F, col 8 ln 63-65, photosite is fully depleted through drain transistor);

a driver configuration unit (2) which controls the transfer of signals in said device;

wherein the photoelectric converting element comprises a buried photodiode (Fig 8) having a charge separating region comprising a first conductivity type high-concentration impurity layer (Fig 8 item p) in an extreme surface of a semiconductor substrate and a charge storing region comprising a second conductivity type impurity layer (Fig 8 item n) in a layer beneath the charge separating region.

4. The claim language "wherein said driver configuration unit is configured such that after the transfer transistor simultaneously transfers the signal charge from all photoelectric converting elements to the charge holding region, an exposure time of the photoelectric converting element starts while the processing unit reads the signal charge from the pixel" describe intended uses of the transfer and drain transistors. Intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of

making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

5. In this case, Fox illustrates the transfer transistor (16), reset transistor (20) and drain transistor (22) have gate nodes (TCK, RST and EC, respectively) that are controlled (by driver unit 2). Simultaneous charge transfer, exposure time, and reading charges from the pixels are all controlled by manipulating the voltages and timing on the gate nodes. Therefore the driver unit and transistors of Fox are capable of functioning as claimed with no modification made to the structure.

6. Regarding claims **2 and 17**, Fox discloses in Fig 1 the device of claims 1 and 16, further having a reset transistor (20) for resetting the charge holding region with a signal charge, and an amplifying transistor (24) for outputting an electric signal corresponding to a potential on the charge holding region, and a selecting transistor (28) for selectively activating the amplifying transistor.

7. With regards to claims **4 and 19**, Fox discloses in Fig 1 the device of claims 1 and 16. The claim language referring to the simultaneous resetting, simultaneous signal transfer, row by row signal read-out, and the fact that the drain transistor is kept on until the reading operation proceeds to a predetermined row, describes an intended use of the device. Intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is

capable of performing the intended use, then it meets the claim. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

8. In this case, Fox illustrates the transfer transistor (16), reset transistor (20) and drain transistor (22) have gate nodes (TCK, RST and EC, respectively) that are controlled (by driver unit 2). Simultaneous charge transfer, exposure time, and reading charges from the pixels are all controlled by manipulating the voltages and timing on the gate nodes. Therefore the driver unit and transistors of Fox are capable of functioning as claimed with no modification made to the structure.

9. With regards to claims **5 and 20**, Fox discloses in Fig 1 the device of claims 4 and 19 wherein the photodiode, after transferring signal charge, includes no charges (col 1 ln 15-17) after readout (by the transfer transistor) or reset (by the drain transistor).

10. Regarding claims **6-8 and 21-23**, Fox discloses the device of claim 4 and 19. In reference to the claim language referring to the voltage applied to the gates of the individual transistors, and that the drain transistor is off during a read operation, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

11. In this case, Fox illustrates the transfer transistor (16), reset transistor (20) and drain transistor (22) have gate nodes (TCK, RST and EC, respectively) that have individual gate voltages applied by the driver unit (2). Therefore the driver unit and

transistors of Fox are capable of functioning as claimed with no modification made to the structure.

12. Regarding claims **27 and 30**, Fox discloses in Fig 1 a solid-state imaging device comprising: a plurality of pixels (Fig 4); each pixels having a light-receiving part (12),

a transfer transistor (16) and gate insulation film (Fig 8, TCK) which reads out a charge in a manner substantially depleting (col 1 ln 15-17) the charge storage region included in the light-receiving part which has a threshold channel potential for turning on the transfer transistor which is set to a value higher than a potential which depletes the light-receiving part (Fig 3B),

a drain transistor (22) and gate insulation film (Fig 8, EC) which drains the charge generated in the light-receiving part, which has a threshold channel potential for turning on the drain transistor which is set to a value higher than a potential which depletes the photoelectric converting element (Fig 3F);

a charge holding region (18) of a second conductivity type (Fig 8 n-type region between TCK and RST) which holds a signal charge,

wherein the light-receiving part has a charge storing region (14) with a potential increasing as the stored charge decreases during reading out charges and during draining charges (Fig 3) but lower than a potential on a channel part in a state the transfer transistor is on and a potential on the channel part in a state the drain transistor is on when the charge storing region is substantially depleted.

13. The claim language "wherein said driver configuration unit is configured such that after the transfer transistor simultaneously transfers the signal charge from all

photoelectric converting elements to the charge holding region, an exposure time of the photoelectric converting element starts while the processing unit reads the signal charge from the pixel" describe intended uses of the transfer and drain transistors.

Intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

14. In this case, Fox illustrates the transfer transistor (16), reset transistor (20) and drain transistor (22) have gate nodes (TCK, RST and EC, respectively) that are controlled (by driver unit 2). Simultaneous charge transfer, exposure time, and reading charges from the pixels are all controlled by manipulating the voltages and timing on the gate nodes. Therefore the driver unit and transistors of Fox are capable of functioning as claimed with no modification made to the structure.

15. With regards to claims **28 and 31**, Fox discloses in Fig 1 the device of claims 27 and 30 wherein the charge storing region, when substantially depleted, includes no charges (col 1 ln 15-17).

16. Regarding claim **29**, Fox discloses in Fig 1 the device of claim 27, wherein the pixel further has a charge holding part (18) for holding a charge read out by the transfer transistor (16). In reference to the claim language referring to the charge being read

simultaneously on all the pixels, the charge being read out in a predetermined order, and the pixels being drained by the drain transistors to start an exposure time period, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963). In this case, a row of the pixel structures of Fox is capable of being read simultaneously, or in a predetermined order, and the drain transistor voids the pixel of unwanted charge (col 1 In 15-17).

17. Regarding claims **32 and 33**, Fox discloses in Fig 1 a solid-state imaging device (col 2 In 1-6) having an imaging region section (10) provided with a plurality of pixels and a processing circuit section for processing an image signal outputted from the imaging region section (col 1 In 20-30), the solid-state imaging device comprising:

- each pixel having a photoelectric converting element (12) for generating a signal charge commensurate with a light-receiving amount,

- a charge holding region (18) of a second conductivity type which holds a signal charge,

- a transfer transistor (16) and gate insulation film (Fig 8, TCK) which transfers a signal charge generated by the photoelectric converting element to the charge holding region, which has a threshold channel potential for turning on the transfer transistor which is set to a value higher than a potential which depletes the light-receiving part (Fig 3B),

a drain transistor (22) and gate insulation film (Fig 8, EC) which drains a signal charge generated by the photoelectric converting element, which has a threshold channel potential for turning on the drain transistor which is set to a value higher than a potential which depletes the photoelectric converting element (Fig 3F);

a reset transistor (20) which resets the charge holding region with a signal charge, and an amplifying transistor (24) which outputs an electric signal corresponding to a potential on the charge holding region, and a selecting transistor (28) which selectively activates the amplifying transistor;

wherein the photoelectric converting element comprises a buried photodiode (Fig 8) having a charge separating region comprising a first conductivity type high-concentration impurity layer (Fig 8 item p) in an extreme surface of a semiconductor substrate and a charge storing region comprising a second conductivity type impurity layer (Fig 8 item n) in a layer beneath the charge separating region; both a channel potential on the drain transistor being turned on and a channel potential on the transfer transistor being turned on are set higher than a potential for depleting the photodiode (Fig 3B for transfer, Fig 3F for drain).

18. The claim language "wherein said driver configuration unit is configured such that after the transfer transistor simultaneously transfers the signal charge from all photoelectric converting elements to the charge holding region, an exposure time of the photoelectric converting element starts while the processing unit reads the signal charge from the pixel" describe intended uses of the transfer and drain transistors. The claim language referring to the simultaneous resetting, simultaneous signal transfer, row

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by row signal read-out, and the fact that the drain transistor is kept on until the reading operation proceeds to a predetermined row, and is off during an operation to read out the signal charge, also describes an intended use of the device.

19. Intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

20. In this case, Fox illustrates the transfer transistor (16), reset transistor (20) and drain transistor (22) have gate nodes (TCK, RST and EC, respectively) that are controlled (by driver unit 2). Simultaneous charge transfer, exposure time, and reading charges from the pixels are all controlled by manipulating the voltages and timing on the gate nodes. Therefore the driver unit and transistors of Fox are capable of functioning as claimed with no modification made to the structure.

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

22. Claims **9 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fox. Fox discloses in Fig 3 an apparatus according to claims 2 and 17, wherein the transfer (16), reset (20) and select (28) transistor are driven on a pixel-row basis (col 5 ln 1-7). Fox does not specify that the transfer, reset and select transistor gate wiring is provided in a row direction while the drain transistor (22) gate wiring is along the column direction, but does disclose that the drain transistor gate wiring is short-circuited together (see timing diagram Figs 4A and 4B).
23. However, it is well known in the art that gate wiring for pixel transistors runs between pixels in either the row or column direction, to be driven by horizontal and vertical scanning circuits. Additionally, Fox discloses a timing diagram in Fig 4B, where the EC signal is held on a column while each row is sampled (transfer, reset, select). It would have been obvious to one of ordinary skill in the art at the time of the invention to arrange the wiring of the transfer, reset and select transistors in the row direction, since they are driven on a row basis, while the drain transistor wiring is arranged along the column direction since it is driven in the vertical direction.
24. Claim **25** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fox and Fossum (US 6,624,456, previously cited). Fox discloses the apparatus of claim 16, but does not specify switch means for switching shutter operation of the imaging device between focal-plane shutter and all-pixel simultaneous shutter operation.

25. Fossum teaches that image sensors may be operated in two ways, one being the rolling shutter (or focal-plane shutter) mode, and the other being an all-pixel simultaneous operation (col 1 ln 12-24), depending on whether the application requires more time consistency. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Fossum on the apparatus of Fox depending on whether the application required more time consistency.

26. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fox and applicant's admitted prior art (AAPA, previously cited). Fox discloses the apparatus of claim 19, but does not specify exposure time selecting means for selecting an exposure time of the device and exposure start row selecting means for selecting the predetermined exposure start row depending on the exposure time selected by the exposure time.

27. However, since Fox has a pixel that is fully depleted during charge transfers, the rows are capable of being selected based on a predetermined exposure time and exposure can be started during readout of signals. It is well known in the art to include exposure time selecting means on cameras. AAPA recites that exposure had been impossible during a transfer duration over all the rows, and therefore exposure time could not be increased. Since Fox is capable of having exposure and readout occurring simultaneously, it would have been obvious to one of ordinary skill in the art at the time of the invention to include exposure time selecting means that select rows for exposure depending on an exposure time selected.

Response to Arguments

28. Applicant's arguments filed 13 July 2010 have been fully considered but they are not persuasive.

29. Regarding the arguments on page 11 that Fox fails to disclose a threshold channel potential for turning on a drain and transfer transistor are higher than a potential which depletes the photoelectric converting element, Fox discloses a transfer transistor (16) and drain transistor (22) with gate nodes (TcK, EC). In Fig 11 Fox illustrates that all charge is drained through the drain transistor, and in Fig 12 Fox illustrates that all charge is transferred through the transfer transistor. As the instant Specification explains, the gate voltage and threshold of the transfer and drain transistors, as well as the dose to the photoelectric element, are adjusted such that the channel potentials on the turned-on drain and transfer transistors are both higher than a potential for depleting the photoelectric element (§79, instant Spec). Due to this, the transfer transistor transfers all of the photoelectrons to the floating diffusion, while the drain transfers all of the photoelectrons onto the drain (§80). Fox illustrates the same result, wherein the transfer transistor transfers all of the photoelectrons to the floating diffusion, while the drain transfers all of the photoelectrons onto the drain. Furthermore, Fox recites that implant doses to the drain and transfer transistors (i.e. threshold voltage), as well as gate voltages, can result in fully voided transistors (i.e. the channel potential for turning on a drain and transfer transistor are higher than a potential which depletes the photoelectric converting element, col 9 ln 18-28). See also column 11 ln 29-49.

Conclusion

30. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN C. INGHAM whose telephone number is (571)272-8793. The examiner can normally be reached on Monday to Friday, 9AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wael M Fahmy/
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Examiner, Art Unit 2814